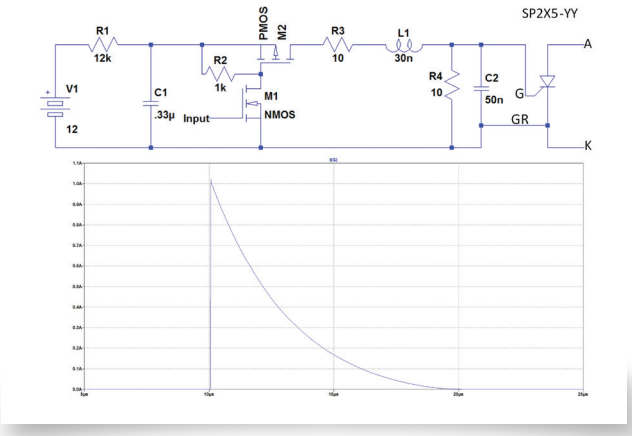
SolidTRON Trigger Example



Theory of Operation

The goal of this trigger circuit is to provide ~1A peak of overdamped gate current having a fast rising edge and lasting for a duration of approximately 10µs.

The fast rising edge (high di/dt) reduces turn-on delay and minimizes jitter. Driving for a duration of 10µs ensures the device stays on for the entire event. In this topology, a low-side NMOS is used to drive a high-side PMOS that provides gate current to a discrete SolidTRON device.

Component Functionality

Part ID	Purpose
V1	Gate drive power supply
R1	Decouples V1 from gate drive, along with C1, sets RC time constant determining mission arming time
C1	Local energy storage for the driver curcuit, along with R3, sets the RC time constant for gate current decay (pulse duration)
R2	Pull-up resistor to keep M2 in off-state, must be large enough to prevent M1 from discharging C1 when M1 is turned on
R3	Current limiting resistor to set peak gate current to ~1A
L1	Lumped model representing stray inductance of entire gate trigger circuit
R4	Keep-off resistor to keep SolidTRON in off-state until triggered
C2	Optional: may be used for increased noise immunity
Input	Sufficient gate signal applied to M1 to initiate trigger sequence

Notes

- C1 and R3 can be changed to accommodate varying supply voltages, exemplary values are in the table to the right
- Lowering the supply voltage will negatively affect the fast rising edge of gate current (di/dt = V/L) so minimizing stray inductance is more important with lower supply voltages RDS-on of M2 can reduce the peak gate current if its value approaches R3 (within 10%)
- Co-packaged solutions are available that contain both M1 and M2, reducing part count
- Selection of M1 and M2 should take into account both V_{TH} and $R_{DS\text{-}on}$ to ensure the MOSFETs will operate in their linear modes with low losses for the selected value of V1

V1 (V)	C1 (µF)	R3 (Ω)
3.3	1.2	2.2
5	1	3.6
12	0.33	10

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